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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,344	11/24/2003	Robert Gentile	500219.02	4725

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EXAMINER	
SHARON, AYAL I	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/722,344	GENTILE ET AL.	
	Examiner	Art Unit	
	Ayal I. Sharon	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *32,34-36,38-40,42-45 and 47-83* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *32,34-36,38-40,42-45 and 47-83* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5)☐ Notice of Informal Patent Application
6)☐ Other: _____.

DETAILED ACTION

Introduction

1. Claims 32, 34-36, 38-40, 42-45, and 47-83 of U.S. Application 10/722,344 are currently pending. The application was filed on 5/24/2004.
2. The application is a continuation of U.S. Application 09/083,959, filed on May 22,1998 (now U.S. Patent 6,654,714).

Claim Objections

3. Claims 50-83 are objected to because of the following informalities: it is not clear whether or not the system claims are directed purely to software. Appropriate correction is required. The applicants have argued that "[t]he MP Configuration Table [taught in the Intel Reference] cannot be a computer implemented method, or software and is not executable code of any kind" (see p.16 of the amendment filed on 5/10/07). In regards to claim 50, a system claim, the applicants further argue that "Intel only teaches or suggests a means of identifying each current processor and storing identifying information in the MP Configuration table."(see p.19 of the amendment filed on 5/10/07).
4. The claims are objected to because it is not clear if the applicants' system claims are directed to "software per se." MPEP § 2106.10 (I) states that "computer programs claimed as computer listings *per se*, i.e., the descriptions or

expressions of the programs, are not physical 'things'", so claims directed to computer programs "*per se*" are not statutory under 35 USC § 101.

5. The applicants are required to clarify this issue.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 36, 45, 57, and 67 recite the limitation "*the computer that is remote from the multiprocessor computer*" or "*the remote computer.*" There is insufficient antecedent basis for this limitation in the claim after the applicants deleted the antecedent basis from the independent claims in the amendment filed 5/10/07.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. The prior art used for these rejections is as follows:

a. Intel MultiProcessor Specification. Version 1.4. May 1997. © 1993-1997. ("**Intel**").

b. Ghori et al., U.S. Patent 5,884,091. Filed: May 24, 1994. Issued: March 16, 1999. ("**Ghori**").

10. Claims 32, 34-35, 38-40, 42-44, 47-56, 58-66, and 68-83 are rejected under 35 U.S.C. 102(a) as being anticipated by Intel.

11. The following discussion of Intel applies to all claims.

12. Intel teaches a Multiprocessor (MP) System Architecture (see Fig.2-1 on p.2-1).

13. Intel also specifically teaches: "While all processors in a complaint system are functionally identical, this specification classifies them into two types: the bootstrap processor (BSP) and the application processors (AP). ... This differentiation is for convenience and is in effect only during the initialization and shutdown processes. The BSP is responsible for initializing the system and booting the operating system; APs are activated only after the system is up and running." (see pp.2-2 to 2-3).

14. Intel also specifically teaches: "The operating system must have access to some information about the multiprocessor configuration. The MP specification teaches two methods for passing this information to the operating system ..." (see p.4-1).

15. Intel also teaches: "The following two data structures are used: (1) The Floating Pointer Structure ... (2) The MP Configuration Table ..." (see p.4-2).

16. Intel also teaches: "The following is a list of the suggested memory spaces for the MP configuration table: (a) In the first kilobyte of Extended BIOS Data Area

(EBDA), or (b) Within the last kilobyte of system base memory if the EBDA segment is undefined, or (c) At the top of system physical memory, or (d) In the BIOS read-only memory space between 0E0000h and 0FFFFFh." (see p.4-2).

17. Intel teaches that the MP Configuration Table includes processor entries (see Table 4-3 on p.4-7), and shows the format of each processor entry (see Fig.4-4 on p.4-7), as well as defining the fields of each processor entry (see Table 4-4 on p.4-8).

18. Intel also teaches that the each processor entry includes a field for "CPUID Feature Flags" (see Table 4-4 on p.4-8). Intel also teaches that one of these flags is for support for the Intel387 floating point instruction set (see Table 4-6 on p.4-9). Each processor entry also includes a field for use of Intel CPU signatures (see Table 4-4 on p.4-8, and Table 4-5 on p.4-9).

19. Intel also teaches that the BSP boots the entire system by accessing the MP configuration table in order to send "wakeup" commands to the APs. (See pp.B-1 to B-3).

20. Finally, Intel teaches: "Some MP operating systems that exist today do not support processors of different types, speeds, or capabilities. However, as processor lifetimes increase and new generations of processors arrive, the potential for dissimilarity among processors increases. The MP specification addresses this potential by providing an MP configuration table to help the operating system configure itself. Operating system writers should factor in processor variations, such as processor type, family, model, and features, to

arrive at a configuration that maximizes overall system performance. At a minimum, the MP operating system should remain operational and should support the common features of unequal processors." (See p.B-7. Emphasis added.)

21. In regards Claim 32, Intel teaches the following limitations:

> *32. (New) A method of selecting a compatible processor for addition to a multiprocessor computer, the multiprocessor computer having at least one current processor and having at least one additional location in which a new processor can be added, the method comprising:*
>
> *storing processor compatibility information, the processor compatibility information identifying processors that are compatible with a plurality of processors that includes each current processor*

(See Intel, especially: p.4-2. "The following is a list of the suggested memory spaces for the MP configuration table: (a) In the first kilobyte of Extended BIOS Data Area (EBDA), or (b) Within the last kilobyte of system base memory if the EBDA segment is undefined, or (c) At the top of system physical memory, or (d) In the BIOS read-only memory space between 0E0000h and 0FFFFFh.")

> *executing a computer program on the multiprocessor computer*

(See Intel, especially: Fig.2-1 on p.2-1; and pp.2-2 to 2-3)

> *directing each of the at least one current processor to execute at least one instruction that allows the identity of each current processor to be determined, the computer program providing identifying information indicative of the identity of each current processor;*

(See Intel, especially: pp.2-2 to 2-3; Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

> *obtaining processor compatibility information indicative of processors that are compatible with a plurality of processors that includes the at least one current processor;*

(See Intel, especially: p.B-7; and Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

> *accessing the stored processor compatibility information to provide accessed processor compatibility information*

executing a computer program comparing the identifying information for each current processor in the multiprocessor computer with the processor compatibility information to determine the processors that are compatible with each current processor; and

(See Intel, especially: p.B-7; and Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

providing information identifying the processors that are compatible with each current processor before adding the new processor to the multiprocessor computer.

(See Intel, especially: p.B-7; and Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

22. Dependent Claims 34-35 and 38-39 are rejected on the same grounds as

Independent claim 32.

23. In regards Claim 40, Intel teaches the following limitations:

40. (New) A method of selecting a compatible processor for addition to a multiprocessor computer, the multiprocessor computer having at least one current processor and having at least one additional location in which a new processor can be added, the method comprising:

storing processor compatibility information, the processor compatibility information identifying processors that are compatible with a plurality of processors that includes at least one current processor;

(See Intel, especially: p.4-2. "The following is a list of the suggested memory spaces for the MP configuration table: (a) In the first kilobyte of Extended BIOS Data Area (EBDA), or (b) Within the last kilobyte of system base memory if the EBDA segment is undefined, or (c) At the top of system physical memory, or (d) In the BIOS read-only memory space between 0E0000h and 0FFFFFh.")

executing a computer program on the multiprocessor computer

(See Intel, especially: Fig.2-1 on p.2-1; and pp.2-2 to 2-3)

directing each of the at least one current processor to execute at least one instruction that allows the identity of each current processor to be determined, the computer program providing identifying information indicative of the identity of each current processor;

(See Intel, especially: pp.2-2 to 2-3; Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

accessing the stored processor compatibility information to provide accessed processor compatibility information;

providing identifying information indicative of the identity of the new processor before adding the new processor to the multiprocessor computer;

(See Intel, especially: p.B-7; and Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

executing a computer program comparing the identifying information for each current processor in the multiprocessor computer with the processor compatibility information to determine the processors that are compatible with each current processor, the computer program further comparing the identifying information for the new processor with the processors determined to be compatible with each current processor; and

(See Intel, especially: p.B-7; and Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

providing an indication whether or not the new processor is compatible before adding the new processor to the multiprocessor computer.

(See Intel, especially: p.B-7; and Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

24. Dependent Claims 42-44 and 47-49 are rejected on the same grounds as Independent claim 40.

25. In regards Claim 50, Intel teaches the following limitations:

50. (New) A system for selecting a new processor for addition to a multiprocessor computer having at least one current processor, the system comprising:

a first component on the multiprocessor computer that determines the identity of each current processor in the multiprocessor computer;

(See Intel, especially: p.B-7; and Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

a second component that stores processor compatibility information indicative of processors that are compatible with a plurality of processors that includes each current processor;

(See Intel, especially: p.4-2. "The following is a list of the suggested memory spaces for the MP configuration table: (a) In the first kilobyte of Extended BIOS Data Area (EBDA), or (b) Within the last kilobyte of system base memory if the EBDA segment is undefined, or (c) At the top of system physical memory, or (d) In the BIOS read-only memory space between 0E0000h and 0FFFFFh.")

a third component coupled to the first and second components to accesses the processor compatibility information using the identity of each current processor in the multiprocessor computer to determine the processors that are compatible with the at least one current processor; and

(See Intel, especially: p.B-7; and Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

a fourth component coupled to the third component that provides information identifying the processors that are compatible with each current processor before adding the new processor to the multiprocessor computer.

(See Intel, especially: p.B-7; and Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

26. Dependent Claims 51-56 and 58-59 are rejected on the same grounds as

Independent claim 50.

27. In regards Claim 60, Intel teaches the following limitations:

60. (New) A system for selecting a new processor for addition to a multiprocessor computer containing at least one current processor, the system comprising:

a first component on the multiprocessor computer that determines the identity of each current processor in the multiprocessor computer;

(See Intel, especially: pp.2-2 to 2-3; Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

a second component allowing identifying information to be provided that identifies the new processor before adding the new processor to the multiprocessor computer;

(See Intel, especially: pp.2-2 to 2-3; Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

a third component that stores processor compatibility information indicative of processors that are compatible with a plurality of processors that includes each current processor;

(See Intel, especially: p.4-2. "The following is a list of the suggested memory spaces for the MP configuration table: (a) In the first kilobyte of Extended BIOS Data Area (EBDA), or (b) Within the last kilobyte of system base memory if the EBDA segment is undefined, or (c) At the top of system physical memory, or (d) In the BIOS read-only memory space between 0E0000h and 0FFFFFh.")

a fourth component coupled to the first, second and third components to compare the identifying information for the new processor with the compatibility information to, determine processors that are compatible with each current processor; and

(See Intel, especially: p.B-7; and Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

a fifth component that provides an indication whether or not the new processor is compatible before adding the new processor to the multiprocessor computer.

(See Intel, especially: p.B-7; and Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

28. Dependent Claims 61-66 and 68-69 are rejected on the same grounds as Independent Claim 60.

29. In regards Claim 70, Intel teaches the following limitations:

70. (New) A computer-readable medium containing instructions for causing a computer system to use processor compatibility information to select a new processor for addition to a multiprocessor computer containing at least one current processor, by:

executing a computer program on the multiprocessor computer

(See Intel, especially: pp.2-2 to 2-3; Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

directing each of the at least one current processor to execute at least one instruction that allows the identity of each current processor to be determined, the computer program providing identifying information indicative of the identity of each current processor;

(See Intel, especially: pp.2-2 to 2-3; Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

obtaining processor compatibility information indicative of processors that are compatible with a plurality of processors that includes the at least one current processor;

(See Intel, especially: p.4-2. "The following is a list of the suggested memory spaces for the MP configuration table: (a) In the first kilobyte of Extended BIOS Data Area (EBDA), or (b) Within the last kilobyte of system base memory if the EBDA segment is undefined, or (c) At the top of system physical memory, or (d) In the BIOS read-only memory space between 0E0000h and 0FFFFFh.")

executing a computer program comparing the identifying information for each current processor in the multiprocessor computer with the processor compatibility information to determine the processors that are compatible with each current processor; and

(See Intel, especially: p.B-7; and Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

providing information identifying the processors that are compatible with each current processor before adding the new processor to the multiprocessor computer.

(See Intel, especially: p.B-7; and Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

30. Dependent Claims 71-75 are rejected on the same grounds as Independent Claim 70.

31. In regards Claim 76, Intel teaches the following limitations:

76. (New) A computer-readable medium containing instructions for causing a computer system to use processor compatibility information to select a new processor for addition to a multiprocessor computer containing at least one current processor, by:

executing a computer program on the multiprocessor computer

(See Intel, especially: pp.2-2 to 2-3; Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

directing each of the at least one current processor to execute at least one instruction that allows the identity of each current processor to be determined, the computer program providing identifying information indicative of the identity of each current processor;

(See Intel, especially: pp.2-2 to 2-3; Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

obtaining processor compatibility information indicative of processors that are compatible with a plurality of processors that includes the at least one current processor;

(See Intel, especially: p.4-2. "The following is a list of the suggested memory spaces for the MP configuration table: (a) In the first kilobyte of Extended BIOS Data Area (EBDA), or (b) Within the last kilobyte of system base memory if the EBDA segment is undefined, or (c) At the top of system physical memory, or (d) In the BIOS read-only memory space between 0E0000h and 0FFFFFh.")

providing identifying information indicative of the identity of the new processor before adding the new processor to the multiprocessor computer;

(See Intel, especially: p.B-7; and Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

executing a computer program comparing the identifying information for each current processor in the multiprocessor computer with the processor compatibility information to determine the processors that are compatible with each current processor, the computer program further comparing the identifying information for the new processor with the processors determined to be compatible with each current processor; and

(See Intel, especially: p.B-7; and Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

providing an indication whether or not the new processor is compatible before adding the new processor to the multiprocessor computer.

(See Intel, especially: p.B-7; and Table 4-4 on p.4-8, and Table 4-5 on p.4-9)

32. Dependent Claims 77-83 are rejected on the same grounds as Independent Claim 76.

33. Claims 32, 34-35, 38-40, 42-44, 47-56, 58-66, and 68-83 are rejected under 35 U.S.C. 102(a) as being anticipated by Ghori.

34. In regards Claim 32, Ghori teaches the following limitations:

32. (New) A method of selecting a compatible processor for addition to a multiprocessor computer, the multiprocessor computer having at least one

current processor and having at least one additional location in which a new processor can be added, the method comprising:

storing processor compatibility information, the processor compatibility information identifying processors that are compatible with a plurality of processors that includes each current processor;

(See Ghori, especially: col.5, lines 30-40. "For example, as part of the boot-up and handshake protocol, the interprocessor communication circuitry 88a of the OEM CPU 10 may store the upgrade family information in a processor register **or at a predetermined memory location**.")

executing a computer program on the multiprocessor computer

(See Ghori, especially: col.3, line 63 to col.4, line 6; and col.5, lines 14-21)

directing each of the at least one current processor to execute at least one instruction that allows the identity of each current processor to be determined, the computer program providing identifying information indicative of the identity of each current processor;

(See Ghori, especially: Fig.3; and col.4, line 62 to col.5, line 12; and col.5, lines 29-54)

accessing the stored processor compatibility information to provide accessed processor compatibility information;

executing a computer program comparing the identifying information for each current processor in the multiprocessor computer with the processor compatibility information to determine the processors that are compatible with each current processor; and

(See Ghori, especially: col.5, lines 29-54; and Fig.2, Item 88a.)

providing information identifying the processors that are compatible with each current processor before adding the new processor to the multiprocessor computer.

(See Ghori, especially: col.5, lines 29-54; and Fig.2, Item 88a. Examiner notes that col.5, lines 52-55 teach that "In that situation [incompatibility], the operating system may choose to not start the upgrade processor and to continue to operate in uniprocessor mode.")

35. Dependent Claims 34-35 and 38-39 are rejected on the same grounds as Independent claim 32.

36. In regards Claim 40, Ghori teaches the following limitations:

40. (New) A method of selecting a compatible processor for addition to a multiprocessor computer, the multiprocessor computer having at least one current processor and having at least one additional location in which a new processor can be added, the method comprising:

storing processor compatibility information, the processor compatibility information identifying processors that are compatible with a plurality of processors that includes each current processor;

(See Ghori, especially: col.5, lines 30-40. "For example, as part of the boot-up and handshake protocol, the interprocessor communication circuitry 88a of the OEM CPU 10 may store the upgrade family information in a processor register **or at a predetermined memory location**.")

executing a computer program on the multiprocessor computer

(See Ghori, especially: col.3, line 63 to col.4, line 6; and col.5, lines 14-21)

directing each of the at least one current processor to execute at least one instruction that allows the identity of each current processor to be determined, the computer program providing identifying information indicative of the identity of each current processor;

(See Ghori, especially: Fig.3; and col.4, line 62 to col.5, line 12; and col.5, lines 29-54)

providing identifying information indicative of the identity of the new processor before adding the new processor to the multiprocessor computer;

(See Ghori, especially: col.5, lines 29-54; and Fig.2, Item 88a. Examiner notes that col.5, lines 52-55 teach that "In that situation [incompatibility], the operating system may choose to not start the upgrade processor and to continue to operate in uniprocessor mode.")

executing a computer program comparing the identifying information for each current processor in the multiprocessor computer with the processor compatibility information to determine the processors that are compatible

with each current processor, the computer program further comparing the identifying information for the new processor with the processors determined to be compatible with each current processor; and

(See Ghori, especially: col.5, lines 29-54; and Fig.2, Item 88a.)

accessing the stored processor compatibility information to provide accessed processor compatibility information

providing an indication whether or not the new processor is compatible before adding the new processor to the multiprocessor computer.

(See Ghori, especially: col.5, lines 29-54; and Fig.2, Item 88a. Examiner notes that col.5, lines 52-55 teach that "In that situation [incompatibility], the operating system may choose to not start the upgrade processor and to continue to operate in uniprocessor mode.")

37. Dependent Claims 42-44 and 47-49 are rejected on the same grounds as

Independent claim 40.

38. In regards Claim 50, Ghori teaches the following limitations:

50. (New) A system for selecting a new processor for addition to a multiprocessor computer having at least one current processor, the system comprising:

a first component on the multiprocessor computer that determines the identity of each current processor in the multiprocessor computer;

(See Ghori, especially: col.3, line 63 to col.4, line 6;
and col.5, lines 14-54)

a second component that stores processor compatibility information indicative of processors that are compatible with a plurality of processors that includes each current processor;

(See Ghori, especially: col.5, lines 30-40. "For example, as part of the boot-up and handshake protocol, the interprocessor communication circuitry 88a of the OEM CPU 10 may store the upgrade family information in a processor register **or at a predetermined memory location**.")

a third component coupled to the first and second components to accesses the processor compatibility information using the identity of each

current processor in the multiprocessor computer to determine the processors that are compatible with the at least one current processor; and

(See Ghori, especially: col.5, lines 29-54; and Fig.3, and associated text at col.4, lines 62-66)

a fourth component coupled to the third component that provides information identifying the processors that are compatible with each current processor before adding the new processor to the multiprocessor computer.

(See Ghori, especially: col.5, lines 29-54; and Fig.2, Item 88a. Examiner notes that col.5, lines 52-55 teach that "In that situation [incompatibility], the operating system may choose to not start the upgrade processor and to continue to operate in uniprocessor mode.")

39. Dependent Claims 51-56 and 58-59 are rejected on the same grounds as

Independent claim 50.

40. In regards Claim 60, Ghori teaches the following limitations:

60. (New) A system for selecting a new processor for addition to a multiprocessor computer containing at least one current processor, the system comprising:

a first component on the multiprocessor computer that determines the identity of each current processor in the multiprocessor computer;

(See Ghori, especially: col.3, line 63 to col.4, line 6;
and col.5, lines 14-54)

a second component allowing identifying information to be provided that identities the new processor before adding the new processor to the multiprocessor computer;

(See Ghori, especially: col.5, lines 29-54; and Fig.2, Item 88a. Examiner notes that col.5, lines 52-55 teach that "In that situation [incompatibility], the operating system may choose to not start the upgrade processor and to continue to operate in uniprocessor mode.")

a third component that stores processor compatibility information indicative of processors that are compatible with a plurality of processors that includes each current processor;

(See Ghori, especially: col.5, lines 30-40. "For example, as part of the boot-up and handshake protocol, the interprocessor communication circuitry 88a of the OEM CPU 10 may store the upgrade family information in a processor register **or at a predetermined memory location**.")

a fourth component coupled to the first, second and third components to compare the identifying information for the new processor with the compatibility information to, determine processors that are compatible with each current processor; and

(See Ghori, especially: col.5, lines 29-54; and Fig.3, and associated text at col.4, lines 62-66)

a fifth component that provides an indication whether or not the new processor is compatible before adding the new processor to the multiprocessor computer.

(See Ghori, especially: col.5, lines 29-54; and Fig.2, Item 88a. Examiner notes that col.5, lines 52-55 teach that "In that situation [incompatibility], the operating system may choose to not start the upgrade processor and to continue to operate in uniprocessor mode.")

41. Dependent Claims 61-66 and 68-69 are rejected on the same grounds as

Independent Claim 60.

42. In regards Claim 70, Ghori teaches the following limitations:

70. (New) A computer-readable medium containing instructions for causing a computer system to use processor compatibility information to select a new processor for addition to a multiprocessor computer containing at least one current processor, by:

executing a computer program on the multiprocessor computer

(See Ghori, especially: col.3, line 63 to col.4, line 6; and col.5, lines 14-21)

directing each of the at least one current processor to execute at least one instruction that allows the identity of each current processor to be

determined, the computer program providing identifying information indicative of the identity of each current processor;

(See Ghori, especially: Fig.3; and col.4, line 62 to col.5, line 12; and col.5, lines 29-54)

obtaining processor compatibility information indicative of processors that are compatible with a plurality of processors that includes the at least one current processor;

(See Ghori, especially: col.5, lines 30-40. "For example, as part of the boot-up and handshake protocol, the interprocessor communication circuitry 88a of the OEM CPU 10 may store the upgrade family information in a processor register **or at a predetermined memory location**.")

executing a computer program comparing the identifying information for each current processor in the multiprocessor computer with the processor compatibility information to determine the processors that are compatible with each current processor; and

(See Ghori, especially: col.5, lines 29-54; and Fig.2, Item 88a.)

providing information identifying the processors that are compatible with each current processor before adding the new processor to the multiprocessor computer.

(See Ghori, especially: col.5, lines 29-54; and Fig.2, Item 88a. Examiner notes that col.5, lines 52-55 teach that "In that situation [incompatibility], the operating system may choose to not start the upgrade processor and to continue to operate in uniprocessor mode.")

43. Dependent Claims 71-75 are rejected on the same grounds as Independent Claim 70.

44. In regards Claim 76, Ghori teaches the following limitations:

76. (New) A computer-readable medium containing instructions for causing a computer system to use processor compatibility information to select a new processor for addition to a multiprocessor computer containing at least one current processor, by:

executing a computer program on the multiprocessor computer

(See Ghori, especially: col.3, line 63 to col.4, line 6; and col.5, lines 14-21)

directing each of the at least one current processor to execute at least one instruction that allows the identity of each current processor to be determined, the computer program providing identifying information indicative of the identity of each current processor;

(See Ghori, especially: Fig.3; and col.4, line 62 to col.5, line 12; and col.5, lines 29-54)

obtaining processor compatibility information indicative of processors that are compatible with a plurality of processors that includes the at least one current processor;

(See Ghori, especially: col.5, lines 30-40. "For example, as part of the boot-up and handshake protocol, the interprocessor communication circuitry 88a of the OEM CPU 10 may store the upgrade family information in a processor register **or at a predetermined memory location**.")

providing identifying information indicative of the identity of the new processor before adding the new processor to the multiprocessor computer;

(See Ghori, especially: col.5, lines 29-54; and Fig.2, Item 88a. Examiner notes that col.5, lines 52-55 teach that "In that situation [incompatibility], the operating system may choose to not start the upgrade processor and to continue to operate in uniprocessor mode.")

executing a computer program comparing the identifying information for each current processor in the multiprocessor computer with the processor compatibility information to determine the processors that are compatible with each current processor, the computer program further comparing the identifying information for the new processor with the processors determined to be compatible with each current processor; and

(See Ghori, especially: col.5, lines 29-54; and Fig.2, Item 88a.)

providing an indication whether or not the new processor is compatible before adding the new processor to the multiprocessor computer.

(See Ghori, especially: col.5, lines 29-54; and Fig.2, Item 88a. Examiner notes that col.5, lines 52-55 teach that "In that situation [incompatibility], the operating system may choose to not start the upgrade processor and to continue to operate in uniprocessor mode.")

45. Dependent Claims 77-83 are rejected on the same grounds as Independent Claim 76.

Response to Arguments

Intel Reference

46. Applicants argue that "[a]lthough the Intel reference generally suggests that the MP Configuration table may be used to allow the operating system to configure itself, Intel does not disclose that such information can be used to determine which if any processors are compatible with existing processors within the system." (See p.17 of the amendment filed 5/10/07).

47. Examiner respectfully disagrees. Intel teaches that among the Base MP Configuration Table Entries, there is an entry for CPU Family and Model. (See Intel: Table 4-5, on page 4-9). Intel further teaches one specific CPU family and model entry that "Indicates a processor that is not an Intel architecture-compatible processor (a graphics controller, for example)." (See Intel: Table 4-5, on page 4-9).

48. Applicants argue that "the Intel reference does not disclose any computer program for providing information about such compatible processors." (See p.17 of the amendment filed 5/10/07).

49. Examiner respectfully disagrees. Intel teaches that:

> A BIOS functions as an insulator between the hardware on one hand, and the operating system and applications software on the other ... For a multiprocessor system, the BIOS may perform the following additional

> functions: * Pass configuration information to the operating system that identifies all processors and other multiprocessing components of the system. (See Intel: Section 2.2 on p.2-5).

While Intel teaches the use of BIOS for this purpose, rather than software, it is old and well known in the art that:

> A central theme of this book that will occur over and over again is:
>
> *Hardware and software are logically equivalent.*
>
> Any operation performed by software can also be built directly into the hardware and any instruction executed by the hardware can also be simulated in software. (See Tanenbaum: p.11)

Therefore, it is a matter of design choice whether the functionality is implemented in hardware or software.

50. Applicants argue that "the Intel reference does not and cannot disclose such a [computer program] method because it only specifies the form and content of the Floating Point Structure and the MP Configuration Table data structures." (See p.17 of the amendment filed 5/10/07).

Examiner respectfully disagrees. See the citation to the Tanenbaum reference immediately above. It is a matter of design choice whether the functionality is implemented in hardware or software.

51. In regards to claim 32, Applicants argue that "[a]lthough Intel does teach a means of identifying each current processor and storing identifying information in the MP Configuration table, it does not teach or suggest any use for such information aside from the general operation of configuring an operating system." (See p.18 of the amendment filed 5/10/07).

52. Examiner respectfully disagrees. The applicant is arguing limitations that do not appear in the claim. Nowhere does the claim recite "using such information aside from the general operation of configuring an operating system." While the claim recites "providing information identifying the processors that are compatible with each current processor before adding the new processor to the multiprocessor computer", Intel teaches that the BIOS provides such information before the processor is added to the multiprocessor computer as a functioning new processor. (See Intel: Table 4-5, on page 4-9). Examiner has given the claimed limitation the broadest reasonable interpretation, and finds that the Intel reference anticipates the limitation.

53. In regards to claim 40, Applicants argue that "Intel does not ... teach or suggest 'providing identifying information indicative of the identity of [a] new processor before adding the new processor to the multiprocessor computer.'" (See pp.18-19 of the amendment filed 5/10/07).

54. Examiner respectfully disagrees. See Intel: Table 4-5, on page 4-9.

55. In regards to claim 40, Applicants also argue that "Intel also does not teach or suggest 'executing a computer program comparing the identifying information for each current processor ... to determine the processors that are compatible with each current processor.'" (See p.19 of the amendment filed 5/10/07).

56. Examiner respectfully disagrees. See Intel: Table 4-5, on page 4-9.

57. In regards to claim 50, Applicants argue that "Intel only teaches or suggests a means of identifying each current processor and storing identifying information in

the MP Configuration table. It does not, however, teach or suggest any use for such information aside from the general operation of configuring an operating system.'" (See p.19 of the amendment filed 5/10/07).

58. Examiner respectfully disagrees. See the response to Applicant's arguments regarding claim 32.

59. In regards to claims 60, 70, and 76, Applicants repeated the arguments presented for the previous claims. (See pp.19-21 of the amendment filed 5/10/07).

Ghori Reference

60. Applicants argue that "Ghori does not disclose any means of identifying existing processors within the system. That is, Ghori only discloses storing identification of the upgrade CPU and not the original CPU." (See p.17 of the amendment filed 5/10/07).

61. Examiner respectfully disagrees. Ghori expressly teaches (emphasis added):

> It is envisioned that operating systems may use the upgrade family information contained in bits 0-3 to further customize system operation. For example, as part of the boot-up and handshake protocol, the interprocessor communication circuitry 88a of the OEM CPU 10 may store the upgrade family information in a processor register or at a predetermined memory location. The operating system can read the stored information and determine that *the upgrade family is the same family as the OEM CPU* (e.g., both are Intel Architecture microprocessors) in which case it will configure the system and operate in a "Homogenous MP" mode. (See Ghori: col.5, lines 29-40)

> Likewise, if the operating system determines the *upgrade processor family type to be different from the family type of the OEM CPU* (e.g., an Intel Architecture and a non-Intel Architecture microprocessors) then it will configure the system and operate in a "Heterogeneous MP" mode. In this case, the operating system may load code compatible with the upgrade processor family type in a separate predetermined memory location where the upgrade processor can execute it. (See Ghori: col.5, lines 40-48)
>
> Alternatively, *in the case of the upgrade and host processor having different family types,* it is possible that the operating system may determine it does not have software compatible with the upgrade processor's family type. In that situation, the operating system may choose to not start the upgrade processor and to continue to operate in uniprocessor mode. (See Ghori: col.5, lines 48-54)

Therefore, it is inherent that Ghori's apparatus stores information of the original CPU.

62. Applicants argue that "Ghori does not disclose a method for determining which processors are compatible with each current processor nor does it disclose communicating that information so that a proper processor may be selected." (See p.17 of the amendment filed 5/10/07).

63. Examiner respectfully disagrees. See the sections of Ghori cited above.

64. In regards to claim 32, Applicants argue that "Although Ghori does teach a means of identifying an upgrade processor and its features, it does not teach or suggest any use for such information aside from the general operation of configuring an operating system." (See p.21 of the amendment filed 5/10/07).

65. Examiner respectfully disagrees. The applicant is arguing limitations that do not appear in the claim. Nowhere does the claim recite "using such information aside from the general operation of configuring an operating system." While the claim recites "providing information identifying the processors that are compatible with

each current processor before adding the new processor to the multiprocessor computer", Ghori teaches that the BIOS provides such information before the processor is added to the multiprocessor computer as a functioning new processor. (See the cited sections of Ghori, above). Examiner has given the claimed limitation the broadest reasonable interpretation, and finds that the Ghori reference anticipates the limitation.

66. In regards to claim 40, Applicants argue that "since Ghori does not teach determining whether a proposed new processor is compatible with existing processors, it likewise does not teach or suggest 'providing identifying information indicative of the identity of [a] new processor before adding the new processor to the multiprocessor computer.'" (See p.22 of the amendment filed 5/10/07).

67. Examiner respectfully disagrees. See the sections of Ghori cited above.

68. In regards to claims 50, 60, 70, and 76, Applicants repeated the arguments presented for the previous claims. (See pp.22-25 of the amendment filed 5/10/07).

Conclusion

69. The following prior art, made of record and not relied upon, is considered pertinent to applicant's disclosure: Andrew S. Tanenbaum. Structured Computer Organization, 2nd Ed. © 1984. pp. 10-12.

70. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action.

71. More specifically, the amendment to independent claims 32, 40, 50, 60, 70, and 76 deleted the limitation that necessitated the inclusion of the Bose and Langan references. The applicants have recognized that Bose and Langan are no longer relevant after the amendment. (See last ¶ of p.17, and first ¶ of p.18 in the amendment filed 5/10/07).

72. All previously applied 35 USC § 103 rejections that included the Bose or Langan references have been changed to 35 USC § 102 rejections, after removing the non-longer-relevant Bose or Langan reference.

73. In addition, the same amendment necessitated the new 35 USC § 112, second paragraph rejections.

74. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

75. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (571) 272-3714. The examiner can normally be reached on Monday through Thursday, and the first Friday of a bi-week, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached at (571) 272-3753.

Any response to this office action should be faxed to (571) 273-8300, or mailed to:

USPTO
P.O. Box 1450
Alexandria, VA 22313-1450

or hand carried to:

USPTO
Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center 2100 Receptionist, whose telephone number is (571) 272-2100.

Ayal I. Sharon
Art Unit 2123
August 3, 2007

PAUL RODRIGUEZ
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100